Sliding Mode Controller in a Multiloop Framework for a Grid-Connected VSI With *LCL* Filter

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***Abstract*—This paper proposes a multiloop framework for current control of grid-connected voltage source inverters (VSIs) with *LCL* output filter. The discrete-time model is of third-order with a nonminimum phase zero when controlling the grid side current. This poses some difficulties on the design of most types of controllers. Motivated by this problem, the inner loop is implemented by a discrete-time sliding mode control law to ensure the tracking of the converter side current. This can be achieved regardless the grid impedance and voltage, making the converter to behave like a current source inverter with a capacitive+inductive (*CL*) filter. Thus, the problem of current control falls from a third-order system to a second-order system. Several types of controllers can be designed to implement the outer loop based on the equivalent *CL* circuit. In this work, a resonant controller with a virtual resistor was applied. Simulations and experimental results are presented to validate the proposal.**

***Index Terms*—*LCL* filter, multiloop control, sliding mode control (SMC).**

I. Introduction

VOLTAGE source inverters (VSIs) are extensively used in the connection of renewable energy sources to the grid. The switching characteristics of this type of converter give rise to a voltage waveform with high-frequency harmonics, and filters must be connected between the converter and the grid to filter these high frequencies out [1]. The two main alternatives are the inductive filter or the *LCL* filter. It is known that for the same harmonic attenuation, a pure inductive filter is bulky if compared with the *LCL* filter and with more reactive power associated, which causes a reduction on its efficiency. Furthermore, the *LCL* filter current control is more complicated due to resonances [2]. Due the advantages in harmonic reduction, the study of *LCL* filter has been a topic of intense research mainly in terms of design guidelines [3] and development of control methods [4]–[10]. The control schemes for grid-connected converters with output filters of *LCL* type include active damping techniques [4], [5], disturbance compensation [6], and robustness with respect to parametric uncertainties [7]–[10]. The main source of *LCL* filter uncertainties is the grid impedance and it may lead to a reduction in the performance of the system or even lead to an unstable operation [11], [12].

One conventional approach for current control widely disseminated in grid-connected converters is the proportional+integral (PI) controller, mainly through the use of *L* filters. However, one has to consider some limitations of this type of controller. Stability issues and poor reference tracking with disturbance compensation are the main drawbacks. The problem gets worse when applying it in the control of *LCL* filters [13], [14]. As an alternative to PI controllers, several strategies have been proposed in the literature. The proportional+resonant (PR) controller has been widely used for reference tracking with harmonic compensation for a given set of harmonics. The combination of the PR controller with the conventional PI controller was addressed in [6] to get the best of each technique in the point of view of disturbance compensation. The control of the weighted average current control is addressed in [15] and [16]. It provides the reduction from a third-order to a first-order system, thus simplifying the control design; however, the dependence on the grid impedance may compromise the performance, mainly in weak grid conditions. The aim of the PR controller is to introduce a high gain at a given frequency, which results in the elimination of the steady-state error [15]. In general, the PR has the main drawback of possible instability as the line impedance increases.

A variety of new emerging and promising techniques for current control of converters have been proposed in the literature [7], [9], [12], [17], [18]. Robust deadbeat approaches were proposed to provide a fast transient response and compensate for the grid-induced current distortions [12]. In [7], an approach is proposed to control the current of a grid-connected VSI using the feedback of the capacitor current of the *LCL* filter. The improvement in the design of the capacitor current feedback gain allows the operation in a wide variation of grid impedance

Manuscript received January 16, 2017; revised May 29, 2017 and August 25, 2017; accepted October 9, 2017. Date of publication November 13, 2017; date of current version February 13, 2018. This work was supported in part by the "Conselho Nacional de Desenvolvimento Científico" and in part by the "Coordenação de Aperfeiçoamento de Pessoal de Nível Superior." *(Corresponding author: Márcio Stefanello.)*

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Digital Object Identifier 10.1109/TIE.2017.2772143

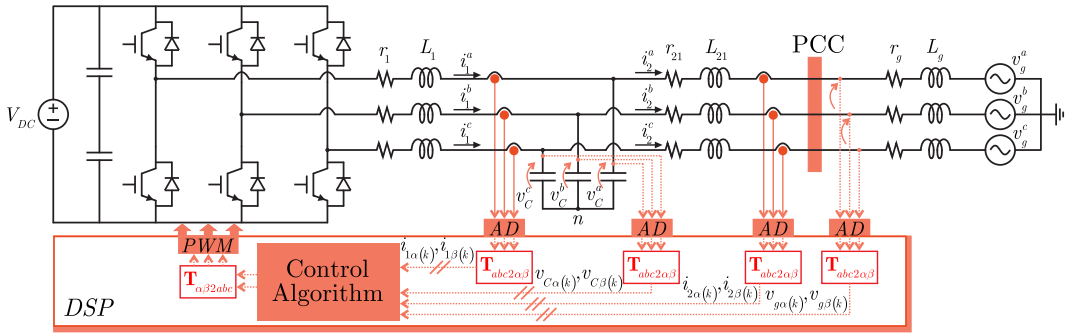


Fig. 1. Three-phase VSI with *LCL* output filter connected in a point of common coupling (PCC) with the grid.

values. The results show the possibility of variation in the grid inductance and an estimation of the total harmonic distortion of the grid current. The main advantages related to this strategy lie on the robustness against parameter uncertainties. It is worth to mention that the control algorithm strongly depends on the design of the *LCL* filter. The choice of the sampling and switching frequencies depends on the *LCL* filter parameters and output power. Some papers that present details of the design procedure of *LCL* filters are [19]–[24].

An important control technique used in systems subject to parameter uncertainties is the sliding mode control (SMC). The variety of application of this method is very wide due to its robustness, associated to simplicity and disturbance rejection capacity. The use of SMC in grid-connected converters is carried out in several papers in the literature [25]–[27]. In [25], an SMC strategy with multiresonant sliding surface aiming the current tracking is presented. The main contribution of the above-mentioned paper is the inclusion of resonant terms of the grid current error in the sliding surface, which results in a good tracking capability. The paper [26] presents an SMC method where the sliding surface is formed by the grid current error, voltage capacitor error, and the derivative of the capacitor voltage error. In [27], a sliding mode controller is combined to a Kalman filter in a three-phase unity power factor rectifier. On the other hand, the discrete-time sliding mode approach is very attractive due to the possibility of easy implementation in digital controllers, and this approach has been developed by several researchers [28]–[30].

In this paper, a multiloop control scheme for current control of a grid-connected VSI with *LCL* output filter is proposed. Two control loops are designed, a fast inner loop is implemented by a discrete-time SMC strategy aiming to track a given current reference in such a way that the closed-loop system operates as a current source driving a capacitive+inductive (*CL*) circuit regardless the grid side impedance and voltage. Thus, the inner control loop makes the converter to behave like a controlled current source. The reference for the inner loop is generated by an outer controller based on a PR controller. At this point, an active damping strategy is included with the feedback of the capacitor voltage. The main feature of the proposed approach is to allow the simplification in the design of the outer loop, which behaves like a second-order system. The paper is organized as follows. Section II presents the modeling and the structure of

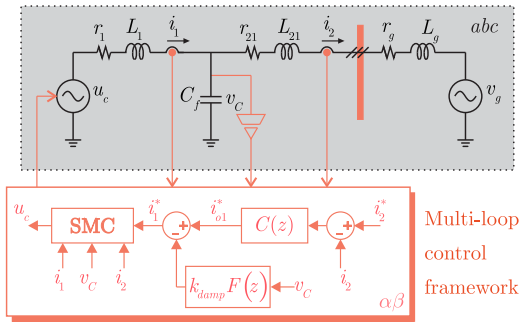


Fig. 2. Single-phase equivalent circuit and controller (*abc* and $\alpha\beta$ stand for the fact that the circuit originates from the electrical coordinates while the controller is implemented in $\alpha\beta$-coordinates).

the system; Section III develops the sliding mode controller; the design of the outer loop is presented in Section IV; and simulation and experimental results are presented in Sections V and VI, respectively. Section VII concludes the paper.

II. System Description

Fig. 1 depicts the system under consideration. It consists of a three-phase VSI connected to the grid through an *LCL* filter. The control algorithm is calculated using a digital signal processor (DSP) in $\alpha\beta$ reference-frame since all three-phase quantities in the natural reference frame were changed to this basis. Thus, the modeling and design will be based on the equivalent circuit of Fig. 2. The voltage u_c is the control action (i.e., the VSI is assumed to have unit gain) synthesized by the SMC. The reference for the converter current is generated by the feedforward of the capacitor voltage v_C through the function $k_{\text{damp}}F(z)$ and by the outer loop controller $C(z)$. This controller is used for asymptotic tracking of the grid current i_2 with compensation of the disturbance v_g.

By defining $r_2 = r_{21} + r_g$, $L_2 = L_{21} + L_g$ from Fig. 2 yields

$$\begin{bmatrix} \dot{i}_1 \\ \dot{v}_C \\ \dot{i}_2 \end{bmatrix} = \begin{bmatrix} -\frac{r_1}{L_1} & -\frac{1}{L_1} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} \\ 0 & \frac{1}{L_2} & -\frac{r_2}{L_2} \end{bmatrix} \begin{bmatrix} i_1 \\ v_C \\ i_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \end{bmatrix} u_c + \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_2} \end{bmatrix} v_g. \tag{1}$$

Applying the Euler discretization method with sampling period T_s from (1) yields

$$\mathbf{x_{1}}_{(k+1)} = \mathbf{G_1}\mathbf{x_{1}}_{(k)} + \mathbf{H_1}u_{c(k)} - \mathbf{H_{d1}}v_{g(k)} \tag{2}$$

where the state vector is $\mathbf{x_1} = \begin{bmatrix} i_1 & v_C & i_2 \end{bmatrix}^T$

$$\mathbf{G_1} = \begin{bmatrix} 1 - \frac{r_1 T_s}{L_1} & -\frac{T_s}{L_1} & 0 \\ \frac{T_s}{C_f} & 1 & -\frac{T_s}{C_f} \\ 0 & \frac{T_s}{L_2} & 1 - \frac{r_2 T_s}{L_2} \end{bmatrix}$$

$\mathbf{H_1} = \begin{bmatrix} T_s/L_1 & 0 & 0 \end{bmatrix}^T$ and $\mathbf{H_{d1}} = \begin{bmatrix} 0 & 0 & T_s\ L_2 \end{bmatrix}^T$.

Accounting for the delay of one sampling period T_s, a fourth state $\phi_{(k)} = u_{c(k-1)}$ is included, yielding the following state-space model:

$$\begin{bmatrix} \mathbf{x_{1}}_{(k+1)} \\ \phi_{(k+1)} \end{bmatrix} = \begin{bmatrix} \mathbf{G_1} & \mathbf{H_1} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \mathbf{x_{1}}_{(k)} \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u_{c(k)} - \begin{bmatrix} \mathbf{H_{d1}} \\ 0 \end{bmatrix} v_{g(k)}$$

$$i_{1(k)} = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \mathbf{x_{1}}_{(k)} \\ \phi_{(k)} \end{bmatrix}. \tag{3}$$

III. Inner Loop: Sliding Mode Control

A. Design of the Discrete-Time Sliding Mode Controller

A discrete-time sliding mode controller is designed to control the converter current i_1. The general procedure in the design is to define a sliding surface and obtain the control signal by manipulating the plant model and the switching function.

The switching function could be defined as the error between the converter current i_1 and its reference i_1^*. Thus

$$\sigma_{(k)} = i_{1(k)} - i^*_{1(k)}. \tag{4}$$

The forward step of switching function is obtained from (4) as

$$\sigma_{(k+1)} = i_{1(k+1)} - i^*_{1(k+1)}. \tag{5}$$

The control action could be obtained by replacing the dynamics of the plant (3) in (5) and solving for $u_{c(k)}$ according to a suitable reaching law. However, due to the inclusion of a delay of one sampling period associated with the digital implementation, the control law $u_{c(k)}$ cannot be obtained directly from $\sigma_{(k+1)}$. In addition, this equation depends on the forward reference $i^*_{1(k+1)}$. In order to solve this problem, the switching function is computed as

$$\sigma_{(k)} = i_{1(k+1)} - i^*_{1(k-1)}. \tag{6}$$

The estimated value for $i_{1(k+1)}$ can be computed from (3) by using the actual measurements. Then, the switching function becomes

$$\sigma_{(k)} = g_1 i_{1(k)} - g_2 v_{C(k)} + g_2 \phi_{(k)} - i^*_{1(k-1)} \tag{7}$$

where $g_1 = 1 - r_1 T_s/L_1$ and $g_2 = T_s/L_1$.

In the design of discrete-time sliding mode controllers, the concept of reaching law plays a fundamental role and it is used to define the behavior of the sliding function given a certain sampling period. The approach applied in this paper was proposed in [28] and is given by

$$\sigma_{(k+1)} - \sigma_{(k)} = -qT_s\sigma_{(k)} - \varepsilon T_s \text{ sign } \left(\sigma_{(k)}\right) \tag{8}$$

where ε and q are positive constants. This law, in particular, defines that the system crosses the switching plane every sampling period once the switching plane is reached.

The expression for $\sigma_{(k+1)}$ is obtained by moving forward the indexes of (6), i.e.,

$$\begin{aligned} \sigma_{(k+1)} &= i_{1(k+2)} - i^*_{1(k)} \\ &= g_1 i_{1(k+1)} - g_2 v_{C(k+1)} + g_2 \phi_{(k+1)} - i^*_{1(k)}. \end{aligned} \tag{9}$$

By replacing the expressions of $i_{1(k+1)}$, $v_{C(k+1)}$, and $\phi_{(k+1)}$ from (3) into (9) yields

$$\begin{aligned} \sigma_{(k+1)} = {} & g_1 \left(g_1 i_{1(k)} - g_2 v_{C(k)} + g_2 \phi_{(k)}\right) \\ & - g_2 \left(\frac{T_s}{C_f} i_{1(k)} + v_{C(k)} - \frac{T_s}{C_f} i_{2(k)}\right) + g_2 u_{c(k)} - i^*_{1(k)}. \end{aligned} \tag{10}$$

Note that the expression of $\sigma_{(k+1)}$ is now dependent on the actual current reference (sample denoted by (k)). Notice that the causality issue was solved by delaying the switching function as shown in (6). The control law is obtained by replacing the expressions (7) and (10) in (8). Thus

$$\begin{aligned} u_{c(k)} = {} & -\frac{L_1}{T_s}\left[c_1 i_{1(k)} - c_2 v_{C(k)} + c_3 \phi_{(k)} + c_4 i_{2(k)}\right. \\ & \left. - i^*_{1(k)} + i^*_{1(k-1)} + qT_s\sigma_{(k)} + \varepsilon T_s \text{ sign } \left(\sigma_{(k)}\right)\right] \end{aligned} \tag{11}$$

where the constants in the above-mentioned equation are given by $c_1 = (g_1^2 - g_1 - g_2\frac{T_s}{C_f})$, $c_2 = g_1 g_2$, $c_3 = (g_1 - 1)g_2$, and $c_4 = g_2\frac{T_s}{C_f}$.

B. Resulting Closed-Loop Dynamics for the Inner Loop

The closed-loop dynamics for the inner loop can be obtained by applying the delayed control law $u_{c(k-1)}$ from (11) in the plant model. The converter current can be modeled as

$$i_{1(k+1)} = g_1 i_{1(k)} - g_2 v_{C(k)} + g_2 u_{c(k-1)} \tag{12}$$

where $u_{c(k-1)}$ is obtained delaying the control law (11) in one sample. Thus

$$\begin{aligned} u_{c(k-1)} = {} & -\frac{L_1}{T_s}\left[c_1 i_{1(k-1)} - c_2 v_{C(k-1)} + c_3 \phi_{(k-1)}\right. \\ & + c_4 i_{2(k-1)} - i^*_{1(k-1)} + i^*_{1(k-2)} + qT_s\sigma_{(k-1)} \\ & \left. + \varepsilon T_s \text{ sign } \left(\sigma_{(k-1)}\right)\right]. \end{aligned}$$

By replacing $u_{c(k-1)}$ in (12) and solving for i_1 yields

$$i_{1(k+1)} = i^*_{1(k-1)} + (1 - qT_s)\,\sigma_{(k-1)} - \varepsilon T_s \text{ sign } \left(\sigma_{(k-1)}\right) \tag{13}$$

where $\sigma_{(k-1)} = i_{1(k)} - i^*_{1(k-2)}$.

From (13), it is possible to conclude about the dynamic behavior of the proposed inner loop based on the sliding mode controller. The output depends on the delayed reference and on the switching band d, which in turn depends on the parameters

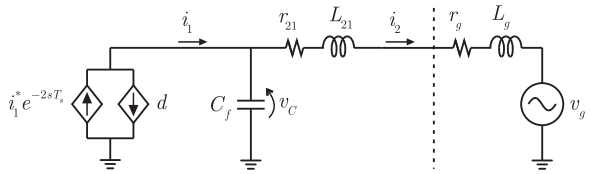


Fig. 3. Equivalent circuit of reduced order obtained from the *LCL* filter when applying the SMC to control the converter current i_1.

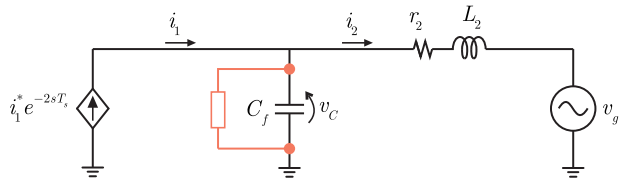


Fig. 4. Equivalent circuit of reduced order with virtual resistor ($r_2 = r_{21} + r_g$ and $L_2 = L_{21} + L_g$. The disturbance d is neglected).

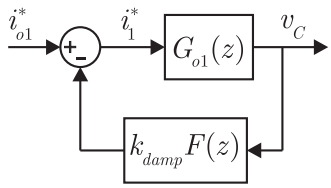


Fig. 5. Block diagram for the design of the active damping gain k_{damp}.

ϵ, q, and T_s. The resulting transfer function of the inner loop is given by

$$i_1(z) = \frac{1}{z^2} i_1^*(z) - d(z) \tag{14}$$

where $d(z) = \varepsilon T_s \ \mathrm{sign}\left(i_1(z) - z^{-2} i_1^*(z)\right)/(z - (1 - qT_s))$.

From (14), it is possible to verify that the choice of the switching function (6) makes the converter current i_1 to track its reference with delay of two samples ($2T_s$). Thus, the inner loop behaves like a current-controlled current source $i_{(k)} = i^*_{1(k-1)}$.

Remark 1: It is worth to mention that some design guidelines can be inferred from (13). Sincea unit gain with wide bandwidth for (14) is necessary , the parameter q can be designed so that $0 < 1 - qT_s \ll 1$. The parameter $\varepsilon > 0$ sets the magnitude of the switching. A big value in the design of ε improves the robustness of the controller; however, it increases the chattering in the i_1 current.

C. Properties of the SMC System

The SMC has the property of ensuring a predefined current behavior according with (14). Replacing $i_{1(k)} = i^*_{1(k-2)} - d_{(k)}$ into (3) results

$$\begin{bmatrix} v_{C(k+1)} \\ i_{2(k+1)} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{T_s}{C_f} \\ \frac{T_s}{L_2} & 1 - \frac{r_2 T_s}{L_2} \end{bmatrix} \begin{bmatrix} v_{C(k)} \\ i_{2(k)} \end{bmatrix} + \begin{bmatrix} \frac{T_s}{C_f} \\ 0 \end{bmatrix} \left(i^*_{1(k-2)} - d_{(k)} \right) + \begin{bmatrix} 0 \\ -\frac{T_s}{L_2} \end{bmatrix} v_{g(k)} \tag{15}$$

where $d_{(k)}$ is the inverse Z-transform of $d(z)$, which is not of interest here because it is a small exogenous disturbance with predefined amplitude.

One can see that (15) is the discrete-time model of the CL circuit depicted in Fig. 3. In other words, the SMC ensures a current-controlled current source behavior for the converter with *LCL* filter when the SMC is used to control the converter current i_1.

The synthesis of the reference current i_1^* is accomplished by an outer loop to achieve some common control objectives, like asymptotic tracking, disturbance compensation, and improvement of the stability margin.

IV. Design of the Outer Loop

This section develops the outer loop controller to generate the reference signal i_1^* for the SMC developed in the previous section.

Many control strategies may be applied to implement the outer loop. Here, a virtual resistor was designed for active damping. A PR controller was designed for asymptotic tracking and disturbance compensation.

A. Active Damping Controller

One of the most simple active damping strategies of resonances for converters with *LCL* filter is the feedback of the current through the capacitor. As a result, a virtual resistor connected in series with the filter capacitor is synthesized. Here, since the inner loop behaves like a current-controlled current source with a *CL* filter, the strategy to design an active damping controller is analogous. The idea is to create an extra reference of current so that the equivalent circuit has a virtual resistor connected in parallel with the filter capacitor, as shown in Fig. 4. The small disturbance $d(z)$ is neglected from this point on without affecting the result.

It is possible to synthesize a virtual resistor feedbacking the voltage through the capacitor for current reference generation, such as

$$i^*_{1(k-2)} = i^*_{o1(k-2)} - k_{\mathrm{damp}} v_{C(k)} \tag{16}$$

where $i^*_{o1(k-2)}$ is the output of the outer loop and it is used to achieve the common control objectives such as asymptotic tracking and stability.

The expression (16) can be rewritten as

$$i^*_{1(k)} = i^*_{o1(k)} - k_{\mathrm{damp}} v_{C(k+2)}. \tag{17}$$

The control (17) synthesizes a perfect virtual resistor. However, it is not possible to obtain the value of $v_{C(k+2)}$ at the time instant $t_{(k)} = kT_s$. Then, we propose the use of a stable filter $F(z)$ with a high bandwidth to feedback the capacitor voltage. This filter uses a pole p_1 for causality, and it is given by

$$F(z) = \frac{z^2}{(z + p_1)^2}. \tag{18}$$

The active damping is implemented according to Fig. 5.

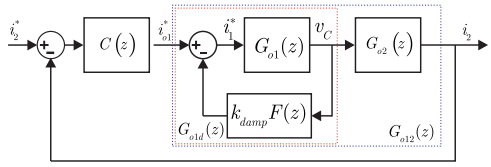


Fig. 6. Block diagram for the overall system including the inner controller (feedback of the voltage v_C) and the outer controller $C(z)$.

The transfer function for the voltage v_C in terms of i_1 is obtained from Fig. 4 and is given by

$$G_{oC}(s) = \frac{v_C(s)}{i_1(s)} = k_{c1}\frac{s+2\zeta\omega_n}{s^2+2\zeta\omega_n s+\omega_n^2} \tag{19}$$

where $\omega_n = 1/\sqrt{L_2C_f}$, $\zeta = r_2\sqrt{C_f/L_2}/2$, and $k_{c1} = 1/C_f$.

Applying the Tustin transform [31] in (19) and since $i_1(z) = i_1^*(z)z^{-2}$ yields

$$G_{o1}(z) = \frac{v_C(z)}{i_1^*(z)} = \frac{1}{z^2}G_{oC}(s)\Big|_{s=\frac{2}{T_s}\frac{z-1}{z+1}} \tag{20}$$

giving rise to

$$G_{o1}(z) = k_{d1}\frac{(z+1)(z-z_{o1})}{z^2(z-p_{o1})(z-p_{o1}^*)} \tag{21}$$

where $k_{d1} = 2T_sk_{c1}(1+\zeta\omega_nT_s)/(T_s^2\omega_n^2+4\zeta\omega_nT_s+4)$, $k_{c1} = 1/C_f$, $z_{o1} = (1-\zeta\omega_nT_s)/(1+\zeta\omega_nT_s)$, and $p_{o1} = (4-T_s^2\omega_n^2+4\omega_nT_s\sqrt{1-\zeta^2}j)/(T_s^2\omega_n^2+4\zeta\omega_nT_s+4)$. p_{o1}^* is the complex conjugated of p_{o1}.

As result, a new transfer function of v_C/i_{o1}^* can be obtained as

$$G_{o1d}(z) = \frac{v_C(z)}{i_{o1}^*(z)} = \frac{G_{o1}(z)}{1+k_{\text{damp}}F(z)G_{o1}(z)}. \tag{22}$$

The design of the damping gain k_{damp} is carried out via the root locus method.

B. Design of the Outer Loop Controller for Asymptotic Tracking and Disturbance Compensation

The block diagram of Fig. 6 illustrates the overall structure of the control system. The current i_2 is used for output feedback in the controller $C(z)$ in order to 1) provide further stability margin; 2) ensure asymptotic tracking of the grid current i_2; and 3) compensate the grid voltage v_g effect.

The model i_2/v_C is given by

$$G_{o2}(s) = \frac{i_2(s)}{v_c(s)} = k_{c2}\frac{1}{s+2\zeta\omega_n} \tag{23}$$

where $k_{c2} = 1/L_2$.

Replacing the Tustin transform yields

$$G_{o2}(z) = \frac{i_2(z)}{v_c(z)} = k_{d2}\frac{z+1}{z-p_{o2}} \tag{24}$$

where $k_{d2} = T_sk_{c2}/(2\zeta\omega_nT_s+2)$ and $p_{o2} = (2-2\zeta\omega_nT_s)/(2+2\zeta\omega_nT_s)$. Notice that p_{o2} is positive and with magnitude smaller than 1.

TABLE I
SYSTEM PARAMETERS FOR SIMULATION AND EXPERIMENTAL RESULTS

Parameter	Value	Parameter	Value
$T_s = T_{\text{sw}}$	$1/12\,000$ s	L_g	1.0 mH
L_1, r_1	1.0 mH, 0.5 Ω	ω_1, ω_g	$2\pi60$ rad/s
L_{21}, r_{21}	0.3 mH, 0.5 Ω	V_g (rms value)	110 V
C_f	62 μF	I_2, ϕ_2^*	7–14 A, 0°

Thus, the overall model for the system is obtained from the cascaded association of $G_{o1d}(z)$ with $G_{o2}(z)$, which results in

$$G_{o12}(z) = G_{o1d}(z)\,G_{o2}(z). \tag{25}$$

The design of the $C(z)$ controller is based on the model (25). A simple PR controller was chosen as follows:

$$C(z) = k_P + C_R(z) \tag{26}$$

where k_P is the proportional gain and $C_R(z)$ is used to achieve asymptotic tracking with disturbance compensation.

1) Design of the PR Controller: The general form of a resonant controller is given by

$$C_{Rh}(s) = k_h\frac{s}{s^2+2\zeta_h\omega_1hs+(h\omega_1)^2} \tag{27}$$

where $0 < \zeta_h \ll 1$ is the damping ratio, ω_1 is the fundamental frequency, and h stands for the order of the harmonic.

Applying the Bilinear transform in (27) results in

$$C_{Rh}(z) = k_{ih}k_1\frac{z^2-1}{z^2-k_1\frac{4-k_2^2}{T_s}z+k_1\frac{4+k_2^2}{T_s}-1} \tag{28}$$

where $k_1 = 2T_s/\left(k_2^2+2\zeta_h2k_2+2^2\right)$ and $k_2 = T_s\omega_1h$.

By considering the tracking with disturbance compensation for other harmonic components, the resonant controller can be written as

$$C_R(z) = \sum_{h=1,\ldots} C_{Rh}(z).$$

The design procedure to obtain the resonant gains are depicted in the next section.

V. DESIGN AND SIMULATION

Simulation and experimental results were obtained for the same plant and controller parameters, which are presented in Table I. The controller for the outer loop can be designed using classical methods, such as root locus or frequency response analysis. In this paper, we use the root locus analysis. The design of the outer loop controllers is presented below.

A. Design Procedure

1) Step 1: Design of the Active Damping Controller: The root locus obtained from the open-loop transfer function $G_{o1d}(z)$ (22) is presented in Fig. 7(a). The filter $F(z)$ has two poles at $z = -0.8$. The gain k_{damp} is designed to improve the damping ratio of the system. The value $k_{\text{damp}} = 0.85$ was selected.

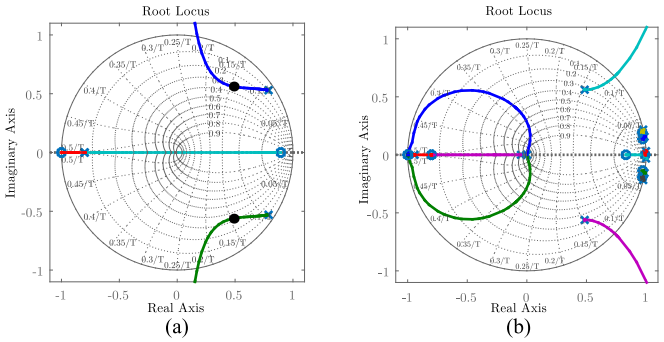


Fig. 7. Plot of the root locus for the design of (a) the active damping gain $k_{\mathrm{damp}} = 0.85$ [with plot using (22)] and (b) the gain of k_P of the PR controller [with plot using (25)].

TABLE II
CONTROLLER GAINS FOR SIMULATION AND EXPERIMENTAL RESULTS

Parameter	Value	Parameter	Value
k_{damp}	0.85	k_{i5}	600
k_P	0.35	k_{i7}	1000
k_{i1}	1500	ε, q	15 000, 11 990

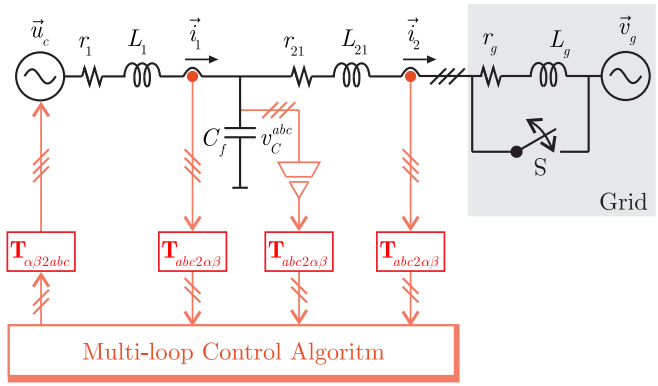


Fig. 8. System considered to obtain the results (the arrow symbol denotes a vector because they are associated with three-phase quantities).

2) Step 2: Design of the PR Controller: The design of the controller $C(z)$ is carried out by the analysis of the open-loop transfer function $G_{o12}(z) = i_2(z)/i_{o1}^*(z)$, given in (25) (see also Fig. 6). The root locus diagram of this system is presented in Fig. 7(b). The gains of $C(z)$ controller are chosen to ensure the margin stability of the system and they are presented in Table II.

B. Simulation Results

Simulation results were obtained in order to demonstrate the performance of the proposed control scheme. The system is depicted in Fig. 8 and the parameters are presented in Table I. The reference current i_2^* in α and β coordinates is given by

$$i_{2\alpha}^* = I_2 \sin\left(\omega_1 t + \phi_{i_{2\alpha}^*}\right) \text{ and } i_{2\beta}^* = I_2 \cos\left(\omega_1 t + \phi_{i_{2\beta}^*}\right) \tag{29}$$

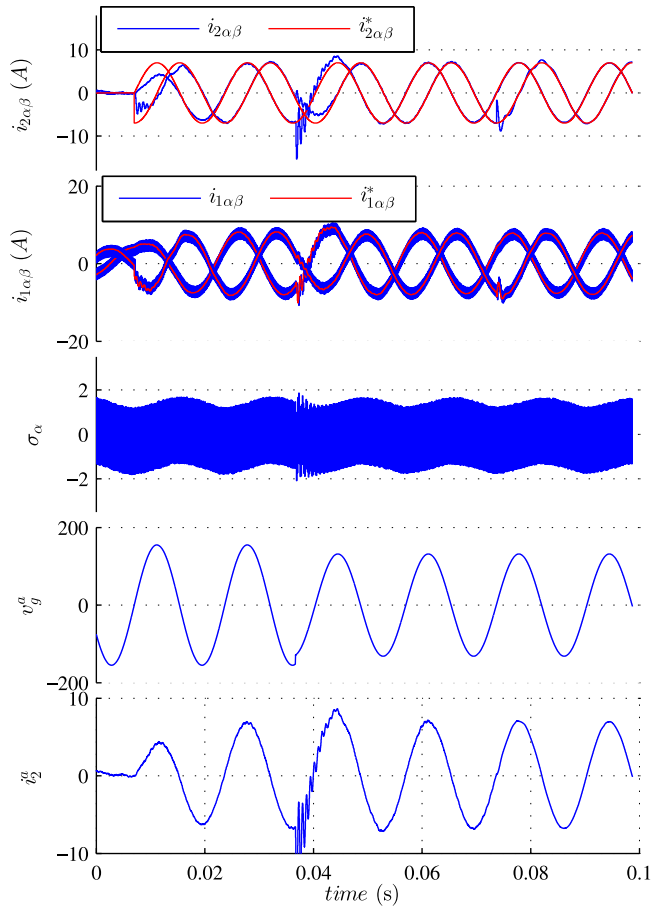


Fig. 9. Simulation results of the proposed current control scheme.

where $\phi_{i_{2\alpha}^*}$ and $\phi_{i_{2\beta}^*}$ are the phase with respect to the α and β components of the grid voltage displaced 90° from each other. The phase values for the grid voltage are given by

$$v_{ga} = V_g \sin(\omega_g t)\,,\ v_{gb} = V_g \sin(\omega_g t - 2\pi/3) \text{ and}$$
$$v_{gc} = V_g \sin(\omega_g t + 2\pi/3)\,.$$

The design of the outer loop (active damping plus PR controllers) presented in Section IV was accomplished from the closed-loop system (15), which in turn was derived from the SMC properties.

The results of Fig. 9 show the performance in terms of tracking of the proposed scheme when the grid voltage v_g and the grid impedance L_g are changed. At the instant $t = 0.038$ s, the grid voltage is reduced to 85% from its rated value. At $t = 0.075$ s, the switch S (see Fig. 8) is turned OFF and an inductance of 1 mH is added to the grid side inductance. It is possible to verify the good tracking of the grid currents $i_{2\alpha\beta}$ in comparison to their references and the good tracking of the converter currents $i_{1\alpha\beta}$ against their references. The switching function σ_α for the α-axis is also presented in Fig. 9. This switching function remains around zero, which demonstrates the tracking capacity of the inner SMC loop. The grid voltage v_g^a and the grid current i_2^a for phase a are also shown in Fig. 9. The inner loop clearly makes the system to behave as expected, i.e., the converter side

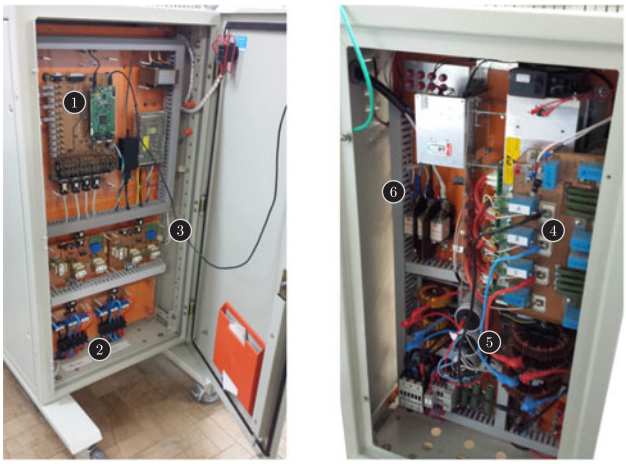


Fig. 10. Experimental setup. (a) Front side and (b) back side of the prototype. (1) DSP. (2) Current transducers and signal conditioning. (3) Voltage sensors and signal conditioning. (4) VSI. (5) *LCL* filter. (6) PCC.

current i_1 tracks its reference i_1^* with a time delay of $2T_s$ plus a switching waveform whose magnitude can be specified.

VI. Experimental Results

In order to verify the performance and robustness of the proposed controller, experimental results were obtained in the laboratory prototype shown in Fig. 10. The controller was implemented in a digital signal processor DSP TMS320F28335 from Texas Instruments. The implemented system is depicted in Fig. 1. The nominal parameters for the experimental system are the same as those used to obtain the simulation results and are presented in Table I. The VSI with *LCL* output filter is connected to the grid through a variable transformer. The phase voltage at point of common coupling (PCC) is 110 V (rms). The VSI operates at a switching frequency of 12 kHz.

According to the previous developments, the performance of the inner control loop based on the SMC is crucial for the design of the outer loop. The converter side current when closing the loop with the SMC was theoretically obtained in Section III-B and verified via simulation in the previous section. Three cases were covered in the experimental results: 1)tracking performance under reference variation; 2) behavior with change in the k_{damp} gain, and 3) stability under grid inductance variation. The results are presented and discussed in the sequel.

A. Performance for a Step Reference for the Grid Current

The reference current i_2^* for α and β coordinates is presented in (29).

The experimental results of Fig. 11 show the grid side current response due to a step on the value of the reference amplitude I_2 [see (29)] from 0 to 7 A in $t = 0.01$ s and then to 12 A in $t = 0.06$ s.

Fig. 11(a) presents the results obtained in the three-phase system, while Fig. 11(b) shows the variables stored in the DSP

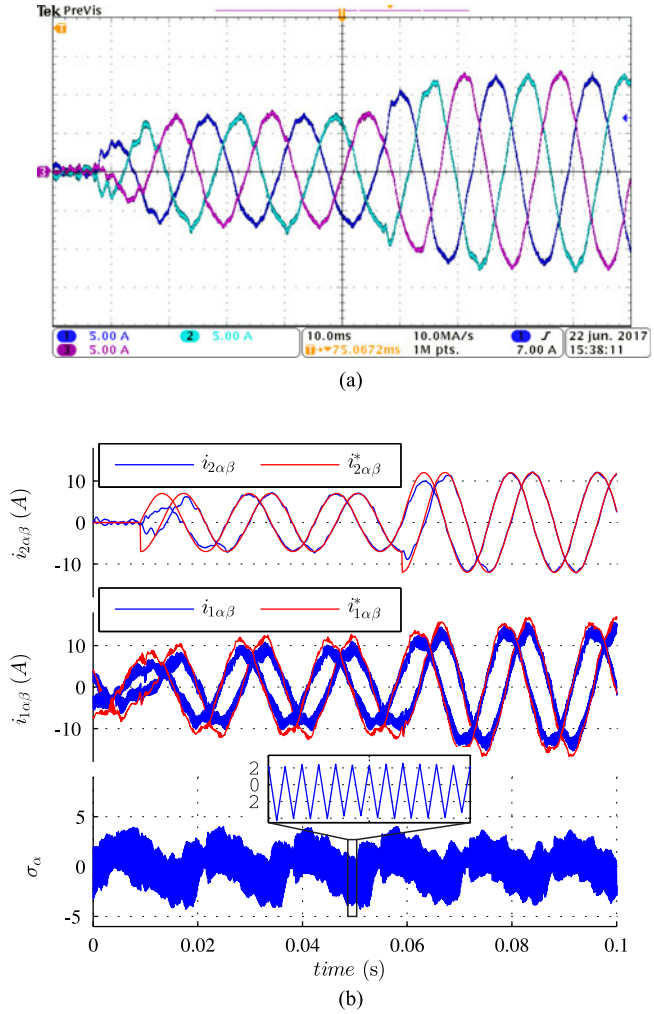


Fig. 11. Reference step of i_2^*. Results for (a) i_2 and (b) to show the tracking performance with the behavior of the switching function σ_α.

in $\alpha\beta$ coordinates to emphasize the tracking and the behavior of the switching function. In the top of Fig. 11(b), it is possible to observe the good convergence of the $i_{2\alpha\beta}$ current to its reference. In the sequel, it is possible to verify the performance of the SMC from the comparison of $i_{1\alpha\beta}$ and $i_{1\alpha\beta}^*$. It is worth pointing out the convergence of the current i_1 to its reference. The computed value of $i_{1(k+1)}$ could be affected by errors in the measurements of currents, voltages, or parametric uncertainties. In this case, the inner loop no longer generates a perfect current source according (14). However, the outer loop can compensate for this effect still tracking the reference i_2^*. The plot in the bottom of Fig. 11(b) is the switching function for the α-axis [see (7)]. We can note that this value is closing zero. There is a zigzag motion around the sliding function switching with the sampling period such as it was designed by expression (8). The magnitude of this band depends on the design of ε, q, and T_s. Fig. 12 presents the control action associated with the results shown in Fig. 11.

B. Influence of the Active Damping Gain

Most active damping strategies are based on the feedback of the current of the capacitor to render an equivalent (and virtual)

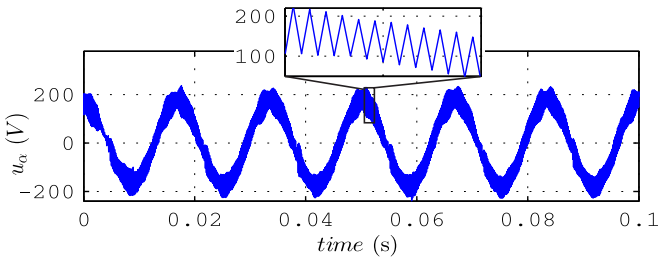
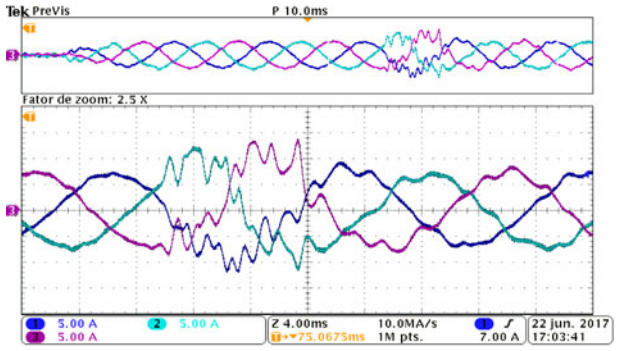
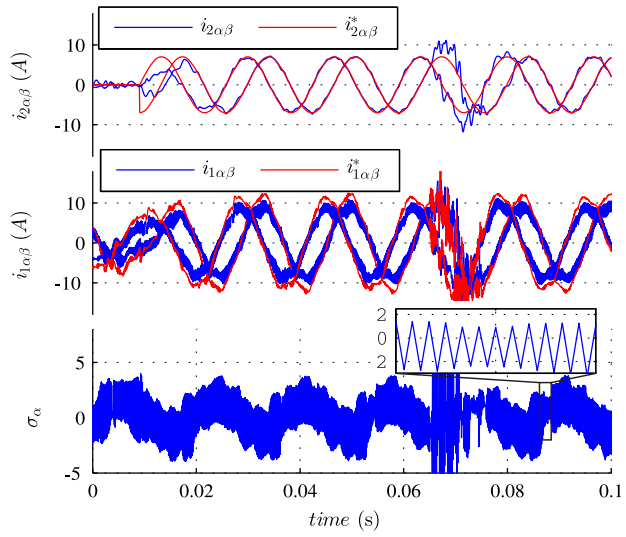


Fig. 12. Control action for the α-axis.



(a)

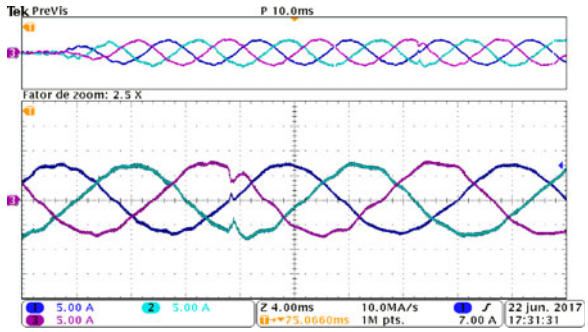


(b)

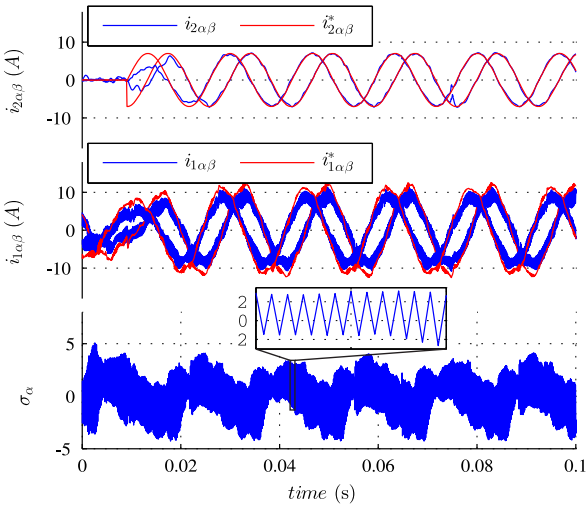
Fig. 13. Reduction of the damping gain k_{damp} from 0.85 to 0.68. (a) Grid-side currents and (b) the tracking performance.

series resistance. In this proposed multiloop approach, instead of feeding back the current, the voltage across the capacitor is used to generate an extra control action in phase with the voltage at the terminals of the capacitor. As a result, an equivalent parallel (and virtual) connected resistor is synthesized.

The experimental results shown in Fig. 13 present the currents when the gain k_{damp} is changed from $k_{\text{damp}} = 0.85$ to 0.68 at $t = 0.06$ s. The three-phase grid currents are shown in Fig. 13(a). It is possible to observe the presence of oscillations in the current when the gain is decreased. To show the behavior of the inner



(a)



(b)

Fig. 14. Change on the grid inductance L_g at $t = 0.73$ s. (a) Three-phase currents i_2. (b) Comparison with the references and the switching function σ.

loop, Fig. 13(b) presents the $\alpha\beta$ components of the converter side current and their references.

C. Stability Under Grid Impedance Change

One of the main concerns in a grid-connected application is to ensure the stability of the closed-loop system even under the uncertainty represented by the grid impedance. The results shown in Fig. 14 present the transient behavior when the grid impedance is increased. Basically, the switch S in the representative scheme of Fig. 8 is turned OFF, thus including the inductor L_g in series with the grid. Fig. 14(a) shows the three-phase current i_2 injected into the grid. It is possible to verify a small distortion in these currents when the inductance is changed. However, the system remains stable with good tracking performance for i_2. The behavior of the inner loop is not affected by the parametric change, as can be verified in Fig. 14(b), and the switching function remains switching around zero, as shown in Fig. 14(b).

VII. Conclusion

In this paper, a multiloop control scheme in discrete-time domain for a grid-connected VSI with an *LCL* filter was

developed. The inner controller was implemented with an SMC for tracking of the converter side current. A good tracking response for this current even with the grid voltage disturbance and impedance uncertainty was demonstrated. More precisely, the converter side current tracked its reference with a fixed delay of two sampling periods of the controller. Thus, the closed-loop system with the SMC behaved like a current-controlled current source inverter with a *CL* filter. Therefore, it had the dynamic behavior of a reduced order system if compared to the third-order of the *LCL* filter. The reference for the inner loop, i.e., the reference for the converter side current, was synthesized by an outer controller. For these tasks, a feedback of the capacitor voltage and a proportional resonant controller were used. Simulation and experimental results were used to validate the proposal.

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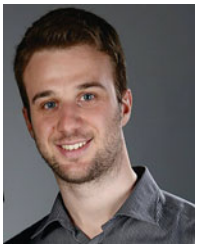

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