SELF-OSCILLATING RESONANT CONVERTER FOR LED APPLICATIONS AT 500 KHZ

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Abstract – **In this paper, an improved design approach is proposed for the self-oscillating command circuit as a driver for resonant converters on LED applications. The improvements, built upon the classic design methodology, contemplate the influence of the MOSFET input capacitance, and make it suitable for high frequency application, where such parasitic elements lead to increased discrepancies. When operated at higher frequencies, resonant converters like the half-bridge series resonant inverter, imply reduced size and weight for the reactive elements, which combined to the simplicity and low cost of the self-oscillating command circuit, translates into a suitable high-power density application. The self-oscillating resonant converter design is based on the describing function method and the extended Nyquist stability criterion, granting the system a proper design prediction around a self-sustained frequency. Simulation and experimental results are shown, comparing the classic design methodology with the improved design approach up to 500 kHz, displaying the feasibility of the design.**

Keywords – **Self-Oscillating, Resonant Converter, LED, High Frequency, Parasitic Capacitances.**

I. INTRODUCTION

Nowadays, resonant converters (RC) offer numerous advantages over ordinary hard-switching electronic systems. Furthermore, resonant converters with soft switching capabilities, when operated in certain frequency ranges, promote a considerable reduction in switching losses. To reduce the size of the reactive elements in RC filters, it is desirable to raise the operating frequency [2], while maintaining good efficiency.

Not until recently, with the development of higher Figure of Merit switching semiconductors like Silicon Carbide (SiC) and Gallium Nitride (GaN), it have been possible to increase the frequency of operation on Power Electronics. Attractive characteristics such as low conduction losses, high switching speed and reduced gate-charge for MOSFET favor a considerable increase in power and frequency for numerous applications, including high-power density lighting applications, like LED drivers.

Fig. 1 shows a self-oscillating resonant converter (SORC) for LED application. The self-oscillating command circuit (SOCC) is a three-winding feedback current transformer with two back-to-back Zener diodes, employed to drive the half-bridge MOSFETs. It is a simple, low cost, robust and reliable circuit that does not require auxiliary DC sources, and has been extensively employed on artificial lighting applications [1][2][3][4], especially in compact fluorescent lamps (CFL), where reduced size and cost are more relevant.

From Fig. 1, the SOCC secondary windings are connected directly to the gate-source of the MOSFETs Q_1 and Q_2, that contains [4] intrinsic capacitances, gate-to-source (C_{GS}) and gate-to-drain (C_{GD}), that hinder the design methodology capability of predicting the SO operating frequency, once their effects on the system are unknown and generally neglected. Thus, to reduce the discrepancy on the chosen oscillating frequency, the gate capacitances have to be properly accounted for, and introduced into the traditional design methodology proposed in [1].

Manufacturers [11][12] state that designers commonly determine component values based only on datasheet information, leading to inadequate design. Although C_{GS} is an important linear parameter, it is crucial to consider the effect of C_{GD}, which is a nonlinear function of the voltage V_{DS} applied to the MOSFET.

A few design methodologies contemplating the intrinsic capacitances of the MOSFET have been proposed in the literature. In [1], an electronic ballast for FL employs the SOCC designed by the describing function method (DFM) and the extended Nyquist criterion (ENC), predicting the SO frequency around a given point and evaluating the presence of a limit cycle [10]. In [2], a more detailed design for the DC-DC SORC is shown, where due to the increase in frequency, the effects of C_{GS} and C_{DS} are considered from a linear point of view. In order to avoid the effect of acoustic resonance in metal halide lamps, the author in [5] proposes a SO electronic ballast operating above 2.65 MHz, where the parasitic effect of the intrinsic capacitances are intensified, becoming a critical point of concern in the design. In [4], the nonlinear effect of both C_{GD} and C_{DS} is analyzed from a simulation perspective, on a 2 W Class-E inverter operating at 4 MHz.

Considering the previous analysis, this paper proposes an improved design procedure for the SOCC. This new procedure takes into account the linear and nonlinear effect of the input capacitances of the MOSFET. Based on this, new analytical expressions for the SOCC are written for the ENC and the DFM.

The paper is organized as follows. Section II presents the SOCC analysis and the capacitor influence on the circuit. Section III focus on the design procedure of the SOCC. Section IV shows experimental results for the SORC. Section V summarizes the main ideas from the paper.

II. ANALYSIS OF THE SELF-OSCILLATING COMMAND CIRCUIT

A. Operational Principles of the SORCC

The operational principles of the SORC from Fig 1Fig. 1, for any given load, albeit Fluorescent Lamps, HPS or LED, is based on the current transformer CT and the two back-to-back diodes. The CT is composed by three windings, being the

primary connected to the output filter, whose primary current I_P is reflected to the secondary windings as I_{S1} and I_{S2} for both MOSFETs input in a complementary way. These currents cause the back-to-back Zener diodes D_{Z1} to D_{Z4} to clamp at the desired gate voltage, driving the HB switches S_1, and S_2, processing the bus voltage E into the output voltage applied to the LED, V_{LED}.
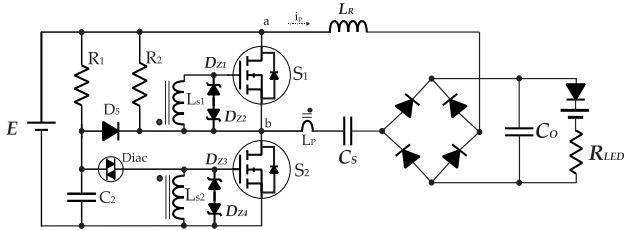

Fig. 1 - Self Oscilating Resonant Converter for LEDs.

Suppressing the effect of the startup circuit R_1/C_2/Diac and representing the complementary HB voltage waveform into a square source varying from zero to the bus voltage E, the simplified circuit for the SORC is shown in Fig. 2. From this circuit, the output filter and load analysis is straightforward. The author in [3] employed this simplified circuit for an electronic ballast, and found an optimal resonant filter, chosen between seven other combinations, favored by desirable features like lamps starting, possibility of soft commutation, DC current absence in the lamp and size of the series and parallel capacitors. For LED applications, however, given the distinction in operating principles of LEDs compared to fluorescent lamps and the voltage characteristics shift from AC to DC, the literature generally presents two filters, the LC series with full-wave rectifier and the LCC series with center tapped transformer and half-wave rectifier [10].

For this paper, the authors chose to drive the LEDs employing the LC filter with full-wave rectifier.
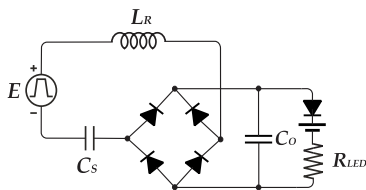

Fig. 2 - LC series resonant filter with full wave rectifier and LED load.

In order to simplify the filter design, the LED, the capacitor and the four diodes from the bridge are replaced by an effective resistive load(see Fig. 3), namely R_{EQ}, calculated through (1), which is dependent of the equivalent resistive value of the chosen LED, extracted from its characteristic curve.
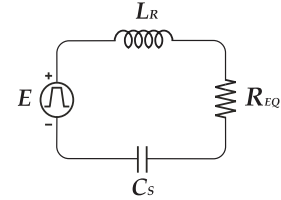
$$R_{EQ} = \frac{8 \cdot R_{LED}}{\pi^2} \tag{1}$$

Fig. 3 - Simplified LC series resonant filter.

Another important parameter is the quality factor Q, where it is shown that this, among other parameters such as bus voltage ripple and switching frequency, greatly affect the ripple transmission from the bus voltage to the LED [10].

According to (3), the quality factor Q is related to the series capacitance C_S and the series inductor L_S from (2). The choice of C_S as an initial parameter results in the value of L_S.

$$L_R = \frac{1}{\omega_R^2 \cdot C_S} \tag{2}$$

$$Q = \sqrt{\frac{L_R}{C_S \cdot R_{EQ}^2}} \tag{3}$$

The required bus voltage to operate the SORC at the chosen frequency is given by (4).

$$E = \frac{\pi^2 \cdot I_{OUT}}{4} \cdot \sqrt{R_{EQ}^2 + \left(\omega \cdot L_R - \frac{1}{\omega \cdot C_S}\right)^2} \tag{4}$$

B. MOSFET Nonlinear Capacitance Behavior and Effects

Fig. 4 shows the physical origin of the parasitic components for an n-channel MOSFET [11][12]. Its operation principle is based on the charge and discharge of these intrinsic capacitances. C_{GS} has a linear dependence of the gate voltage applied, due to the overlap of the source and the polysilicon gate region. C_{GD} exhibits a nonlinear function of the applied voltage, due to the composition of two distinct overlaps, firstly the polysilicon gate and the silicon on the JFET region, and secondly on the depletion region below the gate. Similar to C_{GD}, C_{DS} has a nonlinear dependence of the applied voltage, whose effect is associated with the body-drift diode.
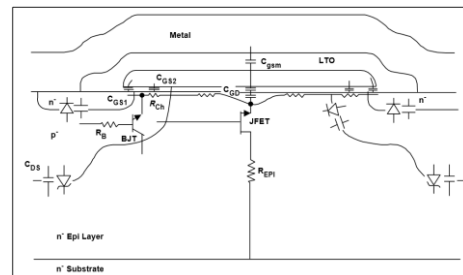

Fig. 4 – Physical origin of parasitic elements on an n-channel MOSFET.

Most papers consider the effect of the MOSFET input capacitances to be linear, giving more attention to C_{GS} and neglecting C_{GD}. However, with a considerable nonlinear effect, C_{GD} makes the sum of the dynamic input capacitances to be higher than the static ones. Called the Miller effect,

stablishes a feedback effect between the input and output of the device.

In contrast to previous methodologies, the SORC design will be enhanced in order to account for both the linear and nonlinear effects of the MOSFET input capacitances in the SOCC design.

C. MOSFET Capacitance Measurement Technique

In order to properly insert the input intrinsic capacitances effect on the SOCC analysis, a method to measure the MOSFET capacitances has to be developed. As it is known, these capacitances depend both on the input and output voltage applied to the MOSFET [12].

The technique presented in this paper consists of measuring the charge delivered to the gate by the drive circuit through the current injected [13]. Mathematically, the capacitance can be calculated through the relationship between the charge delivered to the device and the voltage applied.

Provided an input voltage applied to the gate, one can readily measure the current injected into the gate. The integration of this injected current results in the gate charge, known as the value, in Coulombs, needed to bring a MOSFET into full conduction. The total input capacitance is given by (5).

$$C_{EQ} = \frac{\Delta Q_G}{\Delta V_{GS}} = \frac{\int_{t_0}^{t_1} i_X(t) \times dt}{V_{GS}(t_1) - V_{GS}(t_0)} = \frac{\int_{t_0}^{t_1} I_G(t) \times dt}{V_{GS}(t_1) - V_{GS}(t_0)} \quad (5)$$

D. SOCC Analysis

To design the SORC, the input capacitance effect and the CT model have to combined in a proper way in order to avoid parameter diversion in high frequency operation.

Taking into account the linear effect of C_{GS} and the nonlinear effect of C_{GD} through the measurement method presented previously that results in the total input capacitance C_G, we combine it with the CT model presented in Fig. 5. This model has been thoroughly investigated on previous works on the literature as in [1] and [6], showing its feasibility.
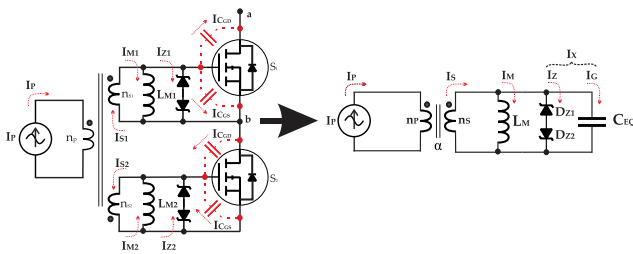
Fig. 5 - (a) Self Oscillating Command Circuit and its (b) simplified version.

Since both secondary windings have the same number of turns, the SOCC can be reduced to its equivalent circuit and reflected to the secondary side, as shown in Fig. 6, with its waveforms shown in Fig. 7. The time from t_0 to t_1 and t_2 to t_3 is the gate-charge period. Here, the current I_G charges C_{GS} and C_{GD}, making V_{GS} vary from $-(V_Z+V_F)$ to $V_Z + V_F$, and vice versa.

From t_1 to t_2, the gate current I_G stops charging the gate, and V_{GS} clamps at the Zener voltage. For ease of analysis, we combine I_Z and I_G into a single sinusoidal current I_X.
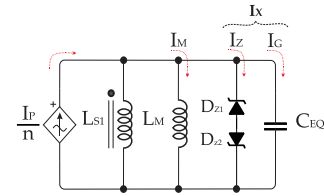
Fig. 6 - Simplified Self Oscillating Command Circuit reflected to the secondary side.

In the traditional design, V_{GS} rise and fall times are neglected, which means that the capacitance does not affect the circuit, disregarding the systems limit in frequency. In the improved design methodology, however, there is a transition time that affect the waveforms considerably, becoming a critical parameter on higher frequencies. Design wise, this time is translated into a phase degree between V_{GS} and the current I_X.
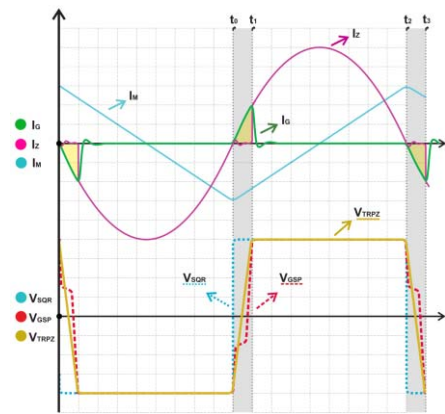
Fig. 7 - SOCC waveforms and gate-to-source V_{GS} voltage representation.

E. SORC Representation

The block diagram shown in Fig. 8a represents the behavior of the SORC from Fig. 1.

The most critical block in this analysis is the hard nonlinearity seen as the $-V_Z/+V_Z$ voltage, that represents the relationship between $I_Z(s)$ and $V_Z(s)$. $G_F(s)$ is the transfer function of the resonant current $I_L(s)$ from the voltage V_{ab}, which represents the behavior of the elements from the LC resonant filter. α_i represents the turns ratio for the CT. $G_M(s)$ is the transfer function that translates the voltage $V_Z(s)$ into the current $I_M(s)$, corresponding to the magnetizing inductance seen at Fig. 6. K represents the proportional relationship between the RC resonant filter input voltage and the gate-to-source voltage $V_Z(s)$.

The block diagram can be reduced, and its simplified version is shown in Fig 8b. The hard nonlinearity is represented by the block N, and similar to [1], the DFM is used to approximately represent its behavior. The block G(s) contains the remainder of the linear part of the system, whose purpose is to pose as a low-pass filter, cutting all harmonics except the fundamental one, applied to the RC resonant filter. G(s) is defined by (6).
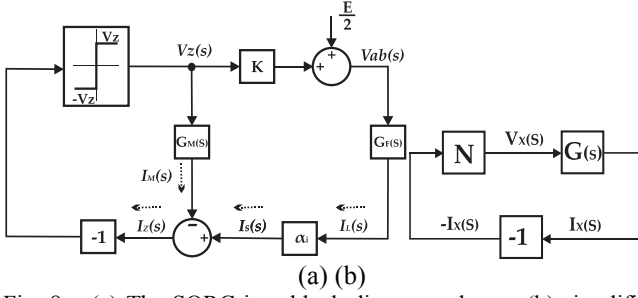
$$G(s) = G_M(s) - K.\alpha_i.G_F(s) \quad (6)$$

Fig. 8 – (a) The SORC in a block diagram scheme; (b) simplified block diagram.

F. Describing Function Method for the Nonlinearity

Traditionally, as seen in [1], the SOCC design is based on the polarity change of V_{GS} of S_1 and S_2, where it is considered as an instant change with no transition times. Although, from the new improved, the key waveforms from Fig. 7 show that it inserts a transition time t_r into the polarity change.

In this way, a new DF that represents the nonlinear effect of the polarity change considering this transition time has to be developed. From the key waveforms of Fig. 7, different approximations for the gate-to-source voltage can be taken into account, where V_{GSP} is the practical value of V_{GS}. Adopting the square waveform approximation, it can be seen that the current I_X, represented as the sum of I_G and I_Z, is not entirely in phase with the square waveform V_{SQR}.

In order to represent the hard nonlinearity with the influence of the capacitance, as a complex gain of the output amplitude, represented by the fundamental voltage of the square wave voltage shown by (7), to the input amplitude, represented by the sinusoidal amplitude of the current I_X, the DF is defined by (8), with a new phase angle (9).

$$V_X = \frac{4 \cdot (V_Z + V_F)}{\pi} \tag{7}$$

$$N(I_X, \omega) = \frac{4 \cdot (V_Z + V_F)}{\pi \cdot I_X} \angle - \varphi(I_X, \omega) \tag{8}$$

$$\phi_{rad}(I_X, C_{GS}, \omega) = a\cos\left\{ \frac{[I_X - 2.(V_Z + V_F).(C_{GS}.\omega)]}{I_X} \right\} \tag{9}$$

III. DESIGN OF THE SELF-OSCILLATING COMMAND CIRCUIT

Special techniques like the ENC are required for a proper SORC design. Considering the existence of a limit cycle for the system with a self-sustained oscillating frequency ω and current amplitude I_X, with $s = j\omega$, the block diagrams reduced (6) and (8), shown in Fig 8b, can be rewritten as (11).

$$1 + NG(s) = 0 \tag{10}$$

$$G(j\omega) = -\frac{1}{N(I_X, \omega)} \tag{11}$$

Applying the ENC, the system will present limit cycles on the conditions that define the interception between $G(j\omega)$ and $N(I_X, \omega)$, shown in Fig. 9. Although the system presents limit cycles on the aforementioned condition, the stability analysis presented in [1] shows that it will only be self-sustained when

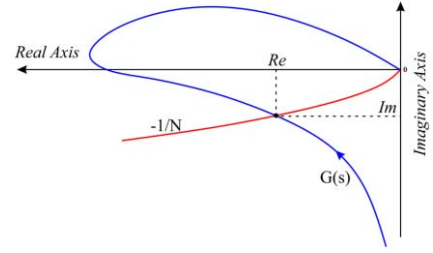$G(j\omega)$ crosses $-1/N(I_X, \omega)$ in clockwise direction [9].

Fig. 9 - Nyquist Diagram.

Furthermore, the phase angle of the DF inserts a nonzero imaginary part on $N(I_X, \omega)$, representing an interception point that no longer occurs on the real axis, as has been shown in previous methodologies, but now on the imaginary part of $G(j\omega)$ and $N(I_X, \omega)$. This translates into an $-1/N(j\omega)$ that has a gate capacitance as a parameter, and evolves further away from the zero imaginary value with the increasing frequency.

A. Design for the SORC using a LC resonant filter

Using LEDs as the load and the LC as a resonant filter, $G_F(s)$ is defined by (12).

$$G_F(j\omega) = \frac{1}{j.\omega.L_S + \dfrac{1}{j.\omega.C_S} + R_{AC}} \tag{12}$$

As shown in Fig. 9, both the real and imaginary part of $G(j\omega)$ and $-1/N(I_X, \omega)$ are equal in the interception point (13). This makes it easy to solve for the amplitude I_X with a simple equaling of both real and imaginary parts.

$$\mathrm{Re}(G(j\omega)) = \mathrm{Re}[-1/N(I_X, j\omega)] \tag{13}$$

With the amplitude of the current I_X, one can find the equation for the magnetizing inductance L_M, given by (18).

$$\mathrm{Im}(G(j\omega)) = \mathrm{Im}[-1/N(I_X, j\omega)] \tag{14}$$

$$\beta = \mathrm{Im}[G_F(j\omega)] \tag{15}$$

$$\zeta = \frac{C_{GS}.\omega.(V_Z + V_F).(C_{GS}.V_F.\omega - I_X(C_{GS}, \omega) + C_{GS}.V_Z.\omega)}{I_X(C_{GS}, \omega)^2} \tag{16}$$

$$\delta(C_{GS}, \omega) = \frac{\pi.I_X(C_{GS}, \omega).\sqrt{-\zeta}}{2.(V_Z + V_F)} \tag{17}$$

$$L_{M1} = -\frac{1}{\omega(\delta(C_{GS}, \omega) + K.\beta.\alpha)} \tag{18}$$

Comparing (18) with other design methodologies like [1] with (19) and [2] with (20), where basically the imaginary part of the DF equals zero, one can see that the improved methodology takes into account the evolution of $-1/N(j\omega)$ based on both the frequency and nonlinear input capacitance effect.

$$L_{M2} = -\frac{1}{K.\beta.\alpha.\omega_s} \qquad (19)$$

$$L_{M3} = -\frac{1}{\omega(\omega.C_{GS} - K.\beta.\alpha.\omega_s)} \qquad (20)$$

IV. EXPERIMENTAL RESULTS

In order to evaluate the improved design procedure for the SORC, experimental results are obtained for three different operating frequencies and three different MOSFETs with distinct capacitances. Being the lower one and therefore having the least impact on parasitic elements, 50 kHz is used as the frequency for the capacitance measurement. The other frequencies are 250 kHz and 500 kHz, selected to further evaluate the feasibility of the method. The results are obtained from a LC resonant filter driving a 10 W LED load with bus voltage of 100 V. Table 1 shows the design parameters, the LC resonant filter components, and the SOCC magnetizing inductances.

The components listed in Table I are presented through their calculated values. However, components with commercially available values equal to the calculated ones, along with the lowest possible tolerance variation were employed (C_S and C_O), reducing the effect of tolerance on the methodology. The deviation on L_R is negligible due to the manufacture process of manual assembly, measured with a high precision LCR meter. If not controlled, these values of tolerance will negatively affect the precision of the high frequency improvement methodology, mainly if a mass-production method is employed for the topology.

Table 1 - SORC Design Parameters

Design Parameters	
Bus Voltage	100 V
Output Power of LEDs	10 W
LED dynamic resistance	24.47 Ω
CT turns ratio	$\alpha_i = 1$
Zener Voltage	12 V
Zener Forward Voltage	1.1 V
MOSFETs	IRF620/640, IPD60R

LC resonant filter			
Frequency f_S	Series Capacitor C_S	Series Inductor L_R	Output Capacitor C_O
50 kHz	12 nF	1160 µH	1 uF
250 kHz	3.3 nF	188 µH	460 nF
500 kHz	1 nF	133 µH	82 nF

SOCC			
	L_{PM}		
Frequency	Proposed Method	Method proposed on [1]	Method proposed on [2]
50 kHz	140 µH	140 µH	140 µH
250 kHz	18.35 µH	28 µH	24.7 µH
500 kHz	7 µH	14 µH	11 µH

According to Table 1, the values for the magnetizing inductance L_{PM} are lower for the proposed method in comparison to the methods proposed on [1] and [2], because it compensates both the linear and nonlinear effects of the input capacitance.

Fig. 10 and Fig. 11 show the gate characteristics for the 50 kHz LC resonant filter, measured on the Vishay IRF640 and the IRF620, respectively. The difference in the gate current (shown in blue) is noticeable, caused by the different input capacitance values, for each MOSFET. The higher the input capacitance, the higher the charge needed to change the MOSFET state, hence the higher gate current.
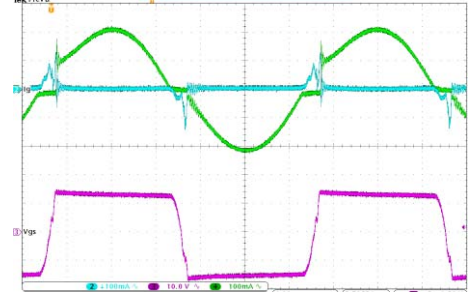

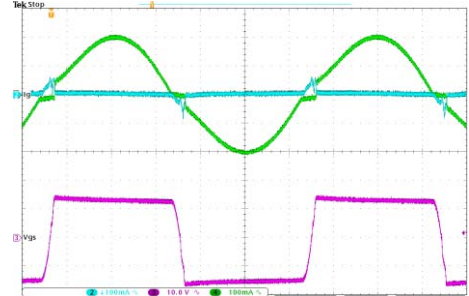Fig. 10 - Gate characteristics (V_{GS}, I_G and I_Z) for the IRF640 at 50 kHz.

Fig. 11 - Gate characteristics (V_{GS}, I_G and I_Z) for the IRF620 at 50 kHz.

Extracting the gate current (blue) and gate voltage (purple) into a CSV file, and afterwards applying the capacitance calculation method, results in the values shown in Table II.

Table 2 - Measured Input Capacitances for different MOSFETs

MOSFET Switches Input Capacitances	
Coolmos IPD60R385CP	1822 pF
IRF640	2000 pF
IRF630	1581 pF
IRF620	1295 pF

After the MOSFETs input capacitances are calculated, the value of L_{PM} is updated. Fig. 12 shows experimental results for the 250 kHz topology using the "Coolmos IPD60R". The system operates at 241 kHz, which compared to the designed frequency, represents an error of only 3.6%.
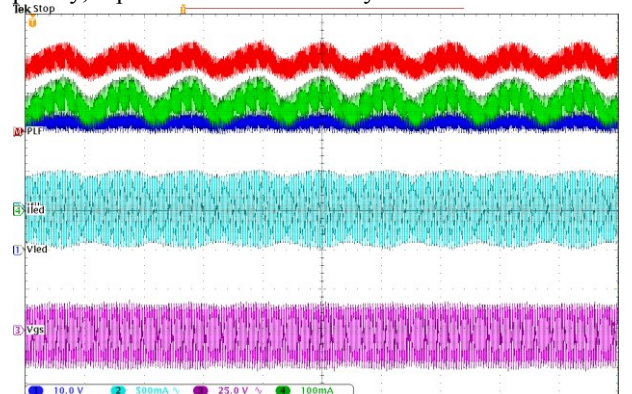
Fig. 12 - Experimental Results for the Coolmos IPD60R at 250 kHz (improved methodology).

Fig. 13 and Fig. 14 show experimental results for the 500 kHz frequency. The first one, designed upon the traditional methodology proposed by [1] operates at 461 kHz, representing an error of 8%. The second operates at 482 kHz, with an error of only 3.6% when compared to the designed frequency. On both waveforms are shown the V_{GS} (purple), the RC filter current I_F (cyan), I_{LED} (green) and V_{LED} (blue) on the LED string, which results in the LED power P_{LED} (red).
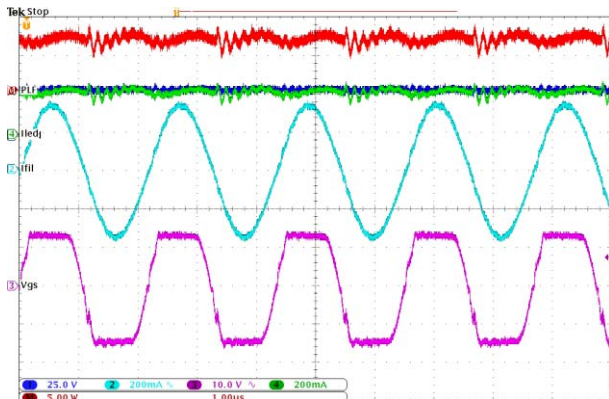

Fig. 13 - Experimental results for the IRF620 at 500 kHz (traditional methodology). Cyan: filter current (200 mA/div); Purple: gate-to-source voltage (10 V/div); Blue and green: voltage and current on the LED string (10 V/div and 100 mA/div). Red: power on the LED (5 W/div).
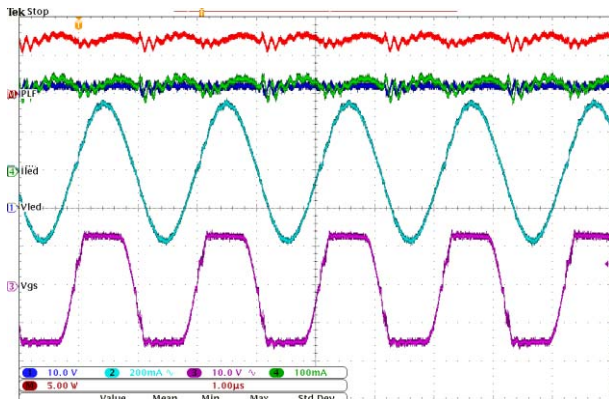

Fig. 14 - Experimental results for the IRF620 at 500 kHz (improved methodology). Cyan: filter current (200 mA/div); Purple: gate-to-source voltage (10 V/div); Blue and green: voltage and current on the LED string (10 V/div and 100 mA/div). Red: power on the LED (5 W/div).

V. CONCLUSION

In contrast to the SOCC traditional methodology, widely employed in the bibliography for low frequency applications, this paper presented an improved design for higher frequencies that takes into account the linear and nonlinear input capacitances of the MOSFET on the SOCC design. The input capacitance measurement technique was employed for three different MOSFETs, clearly exhibiting different levels of gate charge, whose parasitic influence tends to cause errors on the designed oscillating frequency. With the new values for the L_M inserted into the methodology, it was possible to maintain the oscillating frequency error within 3.6% if compared to the designed value, for both 250 kHz and 500 kHz.

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